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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,767	03/29/2004	Thomas R. Keyser	P04,0000 (H0004213,SBE 16	4508

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EXAMINER	
AU, BAC H	

ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/811,767	KEYSER, THOMAS R.	
	Examiner	Art Unit	
	Bac H. Au	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) *32-45* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31 and 46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/7/04; 9/26/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-31 and 46 in the reply filed on February 21, 2006 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-7, 13-14, and 46 are rejected under 35 U.S.C. 102(e) as being anticipated by Patel (U.S. Pub. 2004/0207016).

Regarding claim 1, Patel [Fig.3] discloses a method of making an optoelectronic integrated circuit comprising:

forming isolation trenches [114] in a SOI structure [100] to form at least first [106-A] and second [106-E] isolated areas of silicon;

forming a first silicon island [124] over the first silicon area during a first silicon forming step, wherein the first silicon island forms at least a portion of an optical device [110];

forming a second silicon island [122] over the second silicon area during a second silicon forming step;

processing at least the second silicon area to form an electronic device [108] with the second silicon island;

Regarding claims 2-7, Patel [Para.43] discloses

wherein the first silicon island comprises a poly-silicon island;

wherein the second silicon island comprises a poly-silicon island;

wherein the first silicon island comprises a first poly-silicon island, and wherein the second silicon island comprises a second poly-silicon island;

wherein the first silicon island comprises an amorphous silicon island;

wherein the second silicon island comprises an amorphous silicon island;

wherein the first silicon island comprises a first amorphous silicon island, and wherein the second silicon island comprises a second amorphous silicon island.

Regarding claims 13-14, and 46 Patel [Fig.3] discloses wherein

further comprising vertically etching the SOI structure so as to form a vertical wall of a further optical device [vertically etched sidewall between isolation area 114 and device 112];

wherein the forming of isolation trenches [114] in a SOI structure comprises forming of an isolation trench at least partially filled with a dielectric, and wherein the forming of a first silicon island [124] over the first silicon area comprises forming the first

silicon island over the first silicon area and the dielectric [Active electro-optic device 110];

wherein the first and second silicon forming steps are separate silicon forming steps [Para.42 lines 1-10; para.43 lines 7-14].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 16-22, and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel (U.S. Pub. 2004/0207016) in view of Iwamatsu (U.S. Pub. 2004/0046216).

Regarding claim 16, Patel [Fig.3] discloses a method of making an optoelectronic integrated circuit comprising:

forming isolation trenches [114] in a SOI structure [100] to form at least first [106-A] and second [106-E] isolated areas of silicon;

forming a first silicon island [124] over the first silicon area during a first silicon forming step, wherein the first silicon island forms at least a portion of an optical device [110];

forming a second silicon island [122] over the second silicon area during a second silicon forming step, wherein the first and second silicon forming steps are separate silicon forming steps [Para.42 lines 1-10; para.43 lines 7-14];

processing at least the second silicon area to form an electronic device [108] with the second silicon island; and

siliciding the second portion of the first silicon island [142], at least a portion of the second silicon area [136,140]], and at least of portion of the second silicon island [138] to form contact areas for the optical device and the electronic device.

Patel [Para.44 lines 1-12; para.45 lines 7-11] discloses the selective formation of silicide region 142 on a portion of the first silicon island, but does not explicitly disclose performing this by forming a blocking oxide over a first portion of the first silicon island so as to leave a second portion of the first silicon island exposed. However, Iwamatsu [Fig.64] discloses forming a blocking oxide [IF] over a first portion of the first silicon island so as to leave a second portion of the first silicon island exposed.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Iwamatsu into the method of Patel to include forming a blocking oxide over a first portion of the first silicon island so as to leave a second portion of the first silicon island exposed. The ordinary artisan would have been motivated to modify Patel in the manner set forth above for at least the purpose of forming silicides only in selective regions and preventing silicide formation in regions covered by the oxide [Iwamatsu; para.18].

Regarding claims 17-22, Patel [Para.43] discloses

wherein the first silicon island comprises a poly-silicon island;

wherein the second silicon island comprises a poly-silicon island;

wherein the first silicon island comprises a first poly-silicon island, and wherein the second silicon island comprises a second poly-silicon island;

wherein the first silicon island comprises an amorphous silicon island;

wherein the second silicon island comprises an amorphous silicon island;

wherein the first silicon island comprises a first amorphous silicon island, and wherein the second silicon island comprises a second amorphous silicon island.

Regarding claims 28-30, Patel [Fig.3] discloses the method

further comprising vertically etching the SOI structure so as to form a vertical wall of a further optical device [vertically etched sidewall between isolation area 114 and device 112];

wherein the forming of a blocking oxide comprises forming spacers [128,130] along the second silicon island;

wherein the forming of isolation trenches [114] in a SOI structure comprises forming of an isolation trench at least partially filled with a dielectric, and wherein the forming of a first silicon island [124] over the first silicon area comprises forming the first silicon island over the first silicon area and the dielectric [Active electro-optic device

110].

4. Claims 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel (U.S. Pub. 2004/0207016) in view of Wang (U.S. Pub. 2003/0227058).

Regarding claims 8 and 11, Patel discloses the trenches having vertical side walls, but fails to disclose in the method

wherein the forming of isolation trenches comprises forming LOCOS based dielectric isolation trenches; and

wherein the forming of isolation trenches comprises forming shallow trench dielectric isolation trenches.

However, Wang [Fig.7; para.47] discloses the method wherein the forming of isolation trenches comprises forming LOCOS based dielectric isolation trenches; and wherein the forming of isolation trenches comprises forming shallow trench dielectric isolation trenches.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Wang into the method of Patel to include wherein the forming of isolation trenches comprises forming LOCOS based dielectric isolation trenches; and wherein the forming of isolation trenches comprises forming shallow trench dielectric isolation trenches. The ordinary artisan would have been motivated to modify Patel in the manner set forth above because these methods of forming isolation regions are well-known in the art and are used to provide electrical

and physical separation as well as isolation between active regions [Wang; para.49 lines 1-4].

Regarding claims 9-10, and 12, Patel and Wang disclose the method

further comprising vertically etching the SOI structure so as to form a vertical wall of a further optical device [Patel; Fig.3; vertically etched sidewall between isolation area 114 and device 112];

wherein the LOCOS based dielectric isolation trenches [Wang; 51 of fig.7] have sloped side walls.

5. Claims 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel (U.S. Pub. 2004/0207016) in view of Iwamatsu (U.S. Pub. 2004/0046216) as applied to claim 16 above, and further in view of Wang (U.S. Pub. 2003/0227058).

Regarding claims 23 and 26, Patel and Iwamatsu disclose the trenches having vertical side walls, but fail to disclose in the method

wherein the forming of isolation trenches comprises forming LOCOS based dielectric isolation trenches; and

wherein the forming of isolation trenches comprises forming shallow trench dielectric isolation trenches.

However, Wang [Fig.7; para.47] discloses the method wherein the forming of isolation trenches comprises forming LOCOS based dielectric isolation trenches; and

wherein the forming of isolation trenches comprises forming shallow trench dielectric isolation trenches.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Wang into the method of Patel and Iwamatsu to include wherein the forming of isolation trenches comprises forming LOCOS based dielectric isolation trenches; and wherein the forming of isolation trenches comprises forming shallow trench dielectric isolation trenches. The ordinary artisan would have been motivated to modify Patel and Iwamatsu in the manner set forth above because these methods of forming isolation regions are well-known in the art and are used to provide electrical and physical separation as well as isolation between active regions [Wang; para.49 lines 1-4].

Regarding claims 24-25, and 27, Patel, Iwamatsu, and Wang disclose the method

further comprising vertically etching the SOI structure so as to form a vertical wall of a further optical device [Patel; Fig.3; vertically etched sidewall between isolation area 114 and device 112];

wherein the LOCOS based dielectric isolation trenches [Wang; 51 of fig.7] have sloped side walls.

6. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Patel (U.S. Pub. 2004/0207016) in view of Patel (WO 2004/088396 A2).

Regarding claim 15, '016 fails to disclose in the method wherein the forming of isolation trenches in a SOI structure comprises forming of an isolation trench so as to substantially expose a buried insulation layer of the SOI structure, and wherein the forming of a first silicon island over the first silicon area during a first silicon forming step comprises forming the first silicon island in over the first silicon area and the exposed buried insulation layer. However, '396 [Fig.3] discloses in the method wherein the forming of isolation trenches in a SOI structure comprises forming of an isolation trench so as to substantially expose a buried insulation layer of the SOI structure, and wherein the forming of a first silicon island [10] over the first silicon area [11] during a first silicon forming step comprises forming the first silicon island in over the first silicon area and the exposed buried insulation layer [6].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of '396 into the method of '016 to include wherein the forming of isolation trenches in a SOI structure comprises forming of an isolation trench so as to substantially expose a buried insulation layer of the SOI structure, and wherein the forming of a first silicon island over the first silicon area during a first silicon forming step comprises forming the first silicon island in over the first silicon area and the exposed buried insulation layer. The ordinary artisan would have been motivated to modify '016 in the manner set forth above to form an effective waveguide device where waveguide structures exist in many different arrangements as used in an SOI platform and are well-known in the art ['396; p.5 lines 18-21].

Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Patel (U.S. Pub. 2004/0207016) in view of Iwamatsu (U.S. Pub. 2004/0046216) as applied to claim 16 above, and further in view of Patel (WO 2004/088396 A2).

Regarding claim 31, the rejection is discussed as above in claim 15.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bac H. Au whose telephone number is 571-272-8795. The examiner can normally be reached on Mon-Fri 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BHA

Zandra V. Smith
Supervisory Patent Examiner
19 oct. 2007